REMARKS

The Examiner is thanked for the thorough review and consideration of the present application. The non-final Office Action dated July 18, 2003 has been received and its content carefully reviewed.

By this Response, Applicant has amended Fig. 2 to correct a typographical error, as indicated in red in the annotated sheet showing changes. Claims 1-31 are pending in the application, with claims 11-21 being withdrawn from consideration. Reconsideration and withdrawal of the rejections in view of the above amendments and the following remarks are requested.

In the Office Action, the drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include reference number 22 which was mentioned in the specification. Applicant has amended Fig. 2 to correct the typographical error in which element "22" was incorrectly identified as "21". Accordingly, the objection is overcome.

The Office Action rejected claims 1-4 and 22-25 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,500,702, issued to Lee et al. ("Lee"). Without reaching the substantive merits of cited reference, Applicant traverses the rejection because Lee is not valid prior art against the present application. The filing date of Lee is December 13, 2000. The priority date of the present application is December 27, 1999. Therefore, Applicant respectfully files herewith a certified English translation of Korean Application No. 1999-62983, filed December 27, 1999, to perfect this claim for priority. Withdrawal of the rejection is requested.

The Office Action rejected claims 5-10 and 26-31 under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Applicant's admitted prior art. At the outset, Applicant makes no admittance to prior art. Figures 2 and 4, which have been identified as "admitted prior art" by the Examiner, have been used by the Applicant to provide related art descriptions and have been identified by Applicant in the legend of each applicable figure as "Related Art". Applicant traverses the rejection because Lee is invalid prior art against the present application, and because the Related Art fails to teach or suggest the combined features recited in the claims of the present application. For example, the Related Art fails to teach or suggest a thin film transistor substrate and a liquid crystal display having, among other features, "a protection layer on said source electrode, on a portion of said drain electrode, on said active layer, and on said gate insulation layer, wherein said first side of said drain electrode is covered by said protection

layer and wherein said second side is not covered by said protection layer; and a pixel electrode in electrical contact with the second side of said drain electrode", as recited in independent claims 1 and 22 of the present application.

In the Related Art, as shown in Fig. 3D, "an insulating protection layer 56 is formed over the substrate 1 and over the source and drain electrodes 28 and 30. The protection layer protects the active layer 52. The protection layer is etched to form a drain contact hole 31 that is used to connect the drain electrode 30 to a pixel electrode 14 that is formed later" (Specification, page 6, lines 13-16). However, the Related Art fails to teach or suggest, as illustrated, for example, in Fig. 7D and recited in claims 1 and 22 "a protection layer on said source electrode, on a portion of said drain electrode, on said active layer, and on said gate insulation layer, wherein said first side of said drain electrode is covered by said protection layer, and wherein said second side is not covered by said protection layer; and a pixel electrode in electrical contact with the second side of said drain electrode".

Rejected claims 5-10 and 26-31 depend from independent claims 1 and 22, respectively. By virtue of their dependence from claims 1 and 22, claims 5-10 and 26-31 also contain the allowable subject matter of claims 1 and 22. Because the Related Art fails to teach or suggest the combined features recited in independent claims 1 and 22, rejected dependent claims 5-10 and 26-31 are patentable over the Related Art. Reconsideration and withdrawal of the rejection are requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue. If the Examiner deems that a telephone conversation would further the prosecution of this application, the Examiner is invited to call the undersigned at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed

Dated: October 17, 2003

Respectfully submitted,

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Attachments

Fig.1
(Related Art)

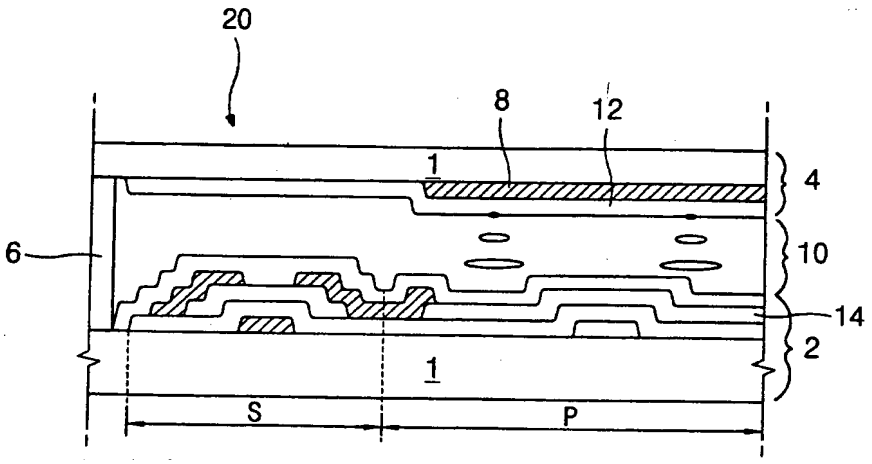
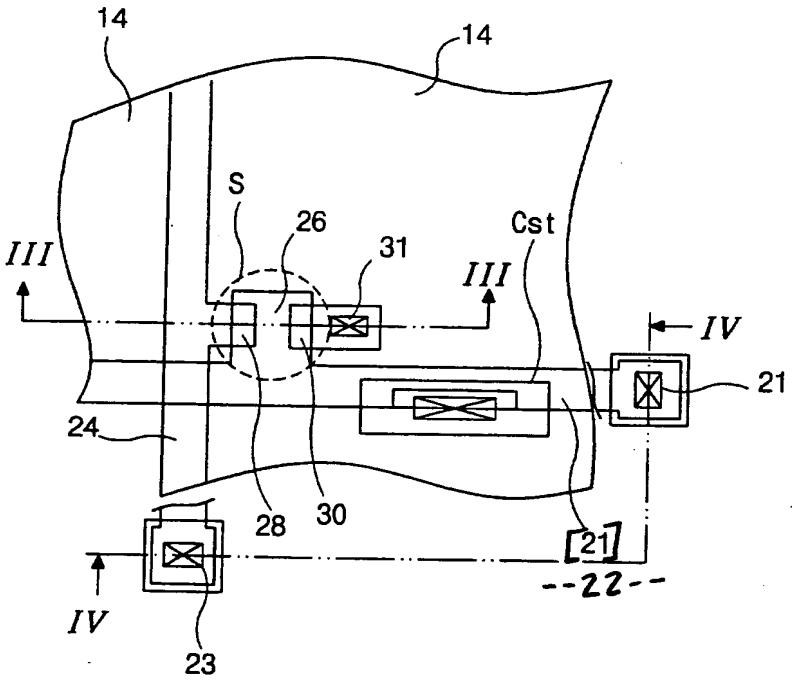


Fig.2
(Related Art)



VERIFICATION OF TRANSLATION

I, Kwang-Won Lee of 114-dong 1103-ho, Hwanggoljugong APT., Yeongtong-dong, Paldal-gu, Suwon-si, Gyeonggi-do, Republic of Korea, declare that I have a thorough knowledge of the Korean and English languages, and the writings contained in the following pages are correct English translation of the specification and claims of Korean Patent Application No. 1999-62983.

This 14th day of October, 2003

By:

Kwang-Won Lee

KOREAN INTELLECTUAL

PROPERTY OFFICE

This is to certify that the following application annexed hereto

is a true copy from the records of the Korean Intellectual Property Office

Application Number : **1999 year Patent Application 62983, PATENT-1999-0062983**

Date of Application : **December 27, 1999**

Applicant(s) : **LG. Philips LCD Co., Ltd.**

COMMISSIONER

[BIBLIOGRAPHICAL DOCUMENTS]

[TITLE OF DOCUMENT] PATENT APPLICATION

[CLSSIFICATION] PATENT

[RECIPIENT] COMMISSIONER OF KOREAN INTELLECTUAL PROPERTY OFFICE

[SUBMISSION DATE] December 27. 1999

[TITLE OF INVENTION IN KOREAN] 액정 표시장치 제조방법 및 그 제조방법에 따른 액정표시장치

[TITLE OF INVENTION IN ENGLISH] LIQUID CRYSTAL DISPLAY AND METHOD FOR FABRICATING THE SAME

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[ATTORNEY CORD] 9-1998-000534-2

[REGISTRATION CORD OF ALL-INCLUSIVE AUTHORIZATION] 1999-001832-7

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[PURPORT] We submit application as above under the article 42 of the Patent Law.

Attorney Jung, Won-Ki (seal)

[FEES]

[BASIC APPLICATION FEE]	20 pages	29,000 Won
[ADDITIONAL APPLICATION FEE]	17 pages	12,000 Won
[PRIORITY FEE]	0 things	0 Won
[EXAMINATION REQUEST FEE]	0 clamis	0 Won
[TOTAL]		41,000 Won

[ENCLOSED] 1. Abstract, Specifications (with Drawings) - 1 set

[DOCUMENT OF ABSTRACT]

[ABSTRACT]

An array substrate for use in a liquid crystal display device incloudes: a substrate having a pixel region and a switching region at one corner of the pixel region; a gate line arranged in a transverse direction on the substrate, a gate electrode extending from the gate line into the switching region, a gate pad at the end of the gate line, and a gate pad electrode over the gate pad; a data line perpendicularly crossing the gate line to define the pixel region, a source electrode extending from the data line over a portion of the gate electrode in the switching region, a data pad at the end of the data line, and a data pad electrode over the data pad; a drain electrode opposite and corresponding to the source electrode in the switching region and overlapping a portions of the gate electrode; a protection layer overlapping the gate electrode, the source electrode, and the drain electrode, and exposing one end portion of the drain electrode; and a pixel electrode contacting the end portion of the drain electrode and disposing over an entire of the pixel region.

[REPRESENTATIVE FIGURE]

FIG. 7D

[SPECIFICATIONS]

[NAME OF INVENTION]

LIQUID CRYSTAL DISPLAY AND METHOD FOR FABRICATING THE SAME

[BRIEF EXPLANATION OF FIGURES]

Fig. 1 is a cross-sectional view illustrating a general liquid crystal display (LCD) panel;

Fig. 2 is a plan view illustrating a pixel of a conventional LCD panel fabricated by using a back exposure and a front exposure;

Figs. 3A to 3E are cross-sectional views taken line III-III of Fig. 2 and illustrate process steps of fabricating a conventional TFT array substrate;

Fig. 4 is a cross-sectional view taken line IV-IV of Fig. 2 and illustrates a gate pad and a data pad according to the conventional art;

Fig. 5 is a flow chart illustrating a manufacturing process of a liquid crystal display device according to the conventional art;

Fig. 6 is a plan view illustrating a pixel of an array substrate according to an embodiment of the present invention;

Figs. 7A to 7D are cross-sectional views taken line VII-VII of Fig. 6 and illustrate process steps of fabricating a TFT array substrate;

Fig. 8 is a cross-sectional view of the TFT array substrate according to the present invention;

Fig. 9 is an enlarged view of a portion "H" of Fig. 8;

Fig. 10 is a cross-sectional view taken along line X-X of Fig. 6 and illustrates a gate pad and a data pad according to the embodiment of the present invention; and

Fig. 11 is a plan view illustrating a gate pad and a data pad according to the principles of the present invention.

<Explanation of major parts in the figures>

100: gate line	102: gate electrode
106: gate pad	108: gate pad electrode
110: data line	112: protection layer
114: source electrode	116: drain electrode
118: data pad	120: data pad electrode
130: pixel electrode	150: gate insulation layer
152: active layer	156: photoresist

[DETAILED DESCRIPTION OF INVENTION]

[OBJECT OF INVENTION]

[TECHNICAL FIELD OF THE INVENTION AND PRIOR ART OF THE FIELD]

The present invention relates to a liquid crystal display device, and more particularly to the liquid crystal display device having thin film transistors (TFTs) and a manufacturing method thereof. In general, a liquid crystal display (LCD) device displays an image using a plurality of pixels. An LCD device that uses thin film transistors (TFTs) as switching elements is typically called a thin film transistor liquid crystal display (TFT-LCD) device.

The liquid crystal display device uses the optical anisotropy and polarization properties of liquid crystal molecules. Because of their peculiar characteristics liquid crystal molecules have a definite orientational order in arrangement. The arrangement direction of liquid crystal molecules can be controlled by an applied electric field. In other words, when electric fields are applied to liquid crystal molecules, the arrangement of the liquid crystal molecules changes. Since incident light is refracted according to the arrangement of the liquid crystal molecules, due to the optical anisotropy of liquid crystal molecules, image data can be displayed.

An active matrix LCD (AM-LCD) has its thin film transistors (TFTs) and pixel electrodes arranged in a matrix. Such LCDs can have high resolution and superior imaging of moving images.

Fig. 1 is a cross-sectional view illustrating a conventional liquid crystal display (LCD) panel. As shown in Fig. 1, the LCD panel 20 has lower and upper substrates 2 and 4 with a liquid crystal layer 10 interposed therebetween. The lower substrate 2, which is referred to as an array substrate, has a TFT "S" as a switching element that changes the orientation of the liquid crystal molecules. A pixel electrode 14 applies a voltage to the liquid crystal layer 10 according to the state of the TFT "S". The upper substrate 4 has a color filter 8 for implementing a color and a common electrode 12 on the color filter 8. The common electrode 12 serves as an electrode for applying a voltage to the liquid crystal layer 10. The pixel electrode 14 is arranged over a pixel portion "P", of a display area. Further, to prevent leakage of the liquid crystal layer 10, the two substrates 2 and 4 are sealed using a sealant 6.

Fig. 2 is a plan view illustrating an array substrate. A gate line 22 is arranged in a transverse direction and a data line 24 is arranged in perpendicular to the gate line 22. A

pixel region having a pixel electrode 14 is defined by the crossing of the gate line 22 and the data line 24.

In an AM-LCD, the switching element (TFT "S") that selectively applies the voltage to the liquid crystal layer 10 (see Fig. 1) is formed near the crossing of the gate line 22 and the data line 24. The TFT "S" has a gate electrode 26 that extends from the gate line 22, a source electrode 28 that extends from the data line 24, and a drain electrode 30 that is electrically connected to the pixel electrode 14 via a contact hole 30'.

A gate pad 21 is formed at one end of the gate line 22, and a data pad 23 is formed at one end of the data line 24. The gate and data pads 21 and 23 are electrically connected with external drive circuitry (not shown) that operates the TFT "S" and thus the pixel electrode 14. The gate line 22 and the pixel electrode 14 form a storage capacitor which stores electric charges.

When the gate line 22 receives gate signals, the TFT "S" is turned ON. The information on the data line 24 is then applied to the pixel electrode 14. The applied electric field from the pixel electrode 14 then changes the arrangement direction of the liquid crystal molecules, causing the liquid crystal molecules to refract the light generated by a back light device. When the gate line 22 turns the TFT "S" to the OFF-state, data signals are not transmitted to the pixel electrode 14. In this case, the arrangement of the liquid crystal is not changed, and thus the direction of the light from back light device is not changed.

When fabricating a liquid crystal panel, a number of complicated process steps are required. In particular, the TFT array substrate requires numerous mask processes. Each mask process requires a photolithography process. Thus, to reduce cost and manufacturing time, the number of mask processes should be minimized.

In general, a manufacturing process depends on the materials used and on the design goals. For example, the resistivity of the material used for the gate lines and the data lines impacts the picture quality of large LCD panels (over 12 inches) and of LCD panels having high resolution. With such LCD panels, a material such as Aluminum (Al) or Al-alloy is often used for the gate lines and the data lines.

In LCD devices having a high aperture ratio, a method of back exposure is employed when forming the pixel electrode 14. That method will now be explained.

Figs. 3A to 3E are cross-sectional views taken along line III-III and illustrate the process steps of fabricating a conventional TFT array substrate for an active matrix LCD device.

An inverted staggered type TFT is generally used due to its simple structure and superior efficiency. The inverted staggered type TFT can be classified as either a back channel etched type (EB) and an etch stopper type (ES), depending on the fabrication method that is used. The fabrication method of the back channel etched type TFT will now be explained.

A first metal layer is deposited on a substrate 1 by a sputtering process. The substrate previously underwent a cleaning process to enhance adhesion between the substrate 1 and the first metal layer. That cleaning process removes organic materials and alien substances from the substrate.

Fig. 3A shows a step of forming a gate electrode 26 by patterning the first metal layer. The gate electrode 26 is usually Aluminum, which reduces the RC delay owing to a low resistance. However, pure Aluminum is chemically weak to and may result in line defects caused by formation of hillocks during a subsequent high temperature process. Thus, an Aluminum alloy or a double-layered structure including Aluminum is beneficially used.

Referring to Fig. 3B, a gate insulation layer 50 is formed over the surface of the substrate 1 and over the gate electrode. Then, a pure amorphous silicon (a-Si:H) layer and a doped amorphous silicon (n+ a-Si:H) layer are formed in sequence on the gate insulation layer 50, and then patterned to form an active layer 55 including a first semiconductor layer 52 and a second semiconductor layer 54. The second semiconductor layer 54 reduces the contact resistance between the active layer 52 and electrodes that will be formed later. The first semiconductor layer 52 is often called as an active layer, and the second semiconductor layer 54 is often called as an ohmic contact layer.

As depicted in Fig. 3C, source and drain electrodes 28 and 30 are formed by depositing and patterning a second metal layer. A portion 54' of the ohmic contact layer is etched using the source and drain electrodes 28 and 30 as masks. If the portion 54' of the ohmic contact layer between the source and drain electrodes 28 and 30 is not removed, serious problems of deteriorated electrical characteristics and low efficiencies of the TFT "S" (see Fig. 2) can result. Etching the portion 54' of the ohmic contact layer over the gate electrode 26 requires special attention. While etching the portion 54' of the ohmic contact layer, the active layer 52 is typically over-etched by about 50~100 nm due to the fact that the active layer 52 and the ohmic contact layer 54 have no etch selectivity.

As shown in Fig. 3D, an insulating protection layer 56 is formed over the substrate 1 and over the source and drain electrodes 28 and 30. The protection layer 56 is etched to form a drain contact hole 30' that is used to connect the drain electrode 30 to a pixel electrode 14a that is formed later.

Due to the unstable energy state of the active layer 52, and due to residual substances that are generated during etching and that can affect the electrical characteristics of the TFT, the protection layer 56 is usually made of an inorganic material, such as silicon nitride (SiN_X)

and silicon oxide (SiO_2), or an organic material such as a BCB (benzocyclobutene). In addition, the protection layer 56 should have a high light transmittance, a high humidity resistance, and a high durability in order to protect the channel area and major portions of a pixel region from humidity damage and scratches that can occur during later process steps.

Fig. 3D also shows a step of forming a pixel electrode 14a by depositing a Transparent Conducting Oxide (TCO) layer and by forming a photoresist PR. Indium Tin Oxide (ITO) or Indium Zinc Oxide (IZO) is usually used for the Transparent Conducting Oxide (TCO) layer. The photoresist PR is a material which, when being subject to light irradiation through a mask, absorbs light energy to cause a photochemical reaction and to form a latent image. To obtain a high aperture ratio, a negative photoresist is preferably used. The portion of the photoresist that does not absorb light is removed during a developing process.

When using a negative photoresist, a back exposure is used in the patterning process. Namely, in the conventional method of fabricating an LCD device, the pixel electrode is formed using a negative photoresist in order to enhance the aperture ratio. With the negative photoresist in place, a back exposure and a front exposure are performed simultaneously to form the pixel electrode. As shown in Fig. 3D, areas B of the photoresist PR are exposed by the back exposure and area F of the photoresist PR is exposed by the front exposure. In the front exposure process, a mask 500 is required for the area F (which is not exposed by the back exposure) to make the pixel electrode 14a have a contact with the drain electrode 30.

Referring to Fig. 3E, a high aperture ratio is produced by the back exposure due to the fact that the area of the pixel electrode 14 is enlarged.

Fig. 4 is a cross-sectional view taken along a line IV-IV of Fig. 2 and illustrates gate and data pads. A gate pad 21 is initially formed on the substrate 1. Then, the gate insulation layer is deposited and then etched to produce a gate pad contact hole that exposes a portion of

the gate pad 21. A data pad 23 is then formed on the gate insulation layer. Then, the protection layer 56, which is patterned to have gate and data pad contact holes that expose the gate and data pads, is formed. Gate and data pad electrodes 62 and 60, which electrically connect to the gate and data pads 21 and 23, via the corresponding contact holes, are then formed on the protection layer 56.

Fig. 5 is a flow chart illustrating the manufacturing process steps of the LCD device as shown in Figs. 3A to 3E.

In the first step, ST200, a glass substrate is cleaned by a cleaning process. That cleaning process enhances adhesion between the substrate and the first metal layer by removing organic materials, alien substances, and particles from the substrate.

In the second step, ST210, the first metal layer, which may be of Aluminum or Molybdenum, is deposited. Then, the gate electrode and a first capacitor electrode, which are portions of the gate line, are formed by lithography process.

In the third step, ST220, the gate insulation layer and the semiconductor layers (the active layer and the ohmic contact layer) are sequentially formed. The gate insulation layer is beneficially comprised of Silicon Oxide or of Silicon Nitride and has a thickness of about 3000 angstroms.

In the fourth step, ST230, the source and drain electrodes are formed by depositing and patterning a metallic material such as Chrome (Cr) or Cr-alloy.

In the fifth step, ST240, a channel region is formed by removing a portion of the doped amorphous silicon layer (ohmic contact layer) between the source and drain electrodes. In this step, the source and drain electrodes are used as masks.

In the sixth step, ST 250, the protection layer is formed to protect the other elements. The protection layer includes contact holes and is made of a material having a high light transmittance, a high humidity resistance, and a high durability.

In the seventh step, ST260, a transparent conductive electrode, beneficially comprised of ITO (Indium-Tin-Oxide) is formed. Then, the pixel electrode is formed by using back and front exposures as previously described. The gate and data pads are also formed in this step.

[TECHNICAL SUBJECT OF INVENTION]

As described above, the prior art requires various masks when fabricating the TFT array substrate of an LCD device, and each mask process requires several steps such as a cleaning step, a depositing step, a baking step and an etching step. Therefore, if the number of mask processes is decreased by only one mask, the throughput and manufacturing yields can dramatically increase and the manufacturing costs and time can be reduced. Furthermore, in the conventional art process of forming pixel electrodes, although a back exposure is used an additional mask for the front exposure is necessary.

To overcome the this problem, the present invention provides a thin film transistor (TFT) array substrate for use in an liquid crystal display (LCD) device that substantially obviates one or more of the problems due to limitations and disadvantages of the related art. Beneficially, such a method increases the throughput and manufacturing yields.

[CONSTRUCTION AND OPERATION OF INVENTION]

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, an array substrate for use in a liquid crystal display device includes: a substrate having a pixel region and a switching region at one

corner of the pixel region; a gate line arranged in a transverse direction on the substrate, a gate electrode extending from the gate line into the switching region, a gate pad at the end of the gate line, and a gate pad electrode over the gate pad; a data line perpendicularly crossing the gate line to define the pixel region, a source electrode extending from the data line over a portion of the gate electrode in the switching region, a data pad at the end of the data line, and a data pad electrode over the data pad; a drain electrode opposite and corresponding to the source electrode in the switching region and overlapping a portions of the gate electrode; a protection layer overlapping the gate electrode, the source electrode, and the drain electrode, and exposing one end portion of the drain electrode; and a pixel electrode contacting the end portion of the drain electrode and disposing over an entire of the pixel region.

The end portion of the drain electrode has a prominence and depression shape. The gate pad includes a gate pad opening and wherein the gate pad electrode contacts side portions of the gate pad in the gate pad opening. The data pad includes a gate pad opening and wherein the data pad electrode contacts side portions of the data pad in the data pad opening. Each of the gate and data pad openings has a prominence and depression shape.

In another aspect, an array substrate for use in a liquid crystal display device includes: a substrate; a gate electrode formed on the substrate; a gate insulation layer on the substrate to cover the gate electrode; an active layer on the gate insulation layer and over the gate electrode; source and drain electrodes contacting the active layer; a protection layer covering the active layer and the source electrode, and exposing a portion of the drain electrode; and a pixel electrode contacting side portions of the drain electrode. The pixel electrode overlaps the side portions of the drain electrode by a distance of less than 2 micrometers.

In another aspect, a method of forming an array substrate for use in a liquid crystal display device includes: providing a substrate; forming a gate electrode on the substrate;

forming a gate insulation layer on the substrate to cover the gate electrode; forming an active layer on the gate insulation layer and above the gate electrode, wherein the active layer includes a pure amorphous silicon layer and a doped amorphous silicon layer; forming source and drain electrodes on the active layer; forming a channel region between the source and drain electrodes; forming a protection layer over an entire of the substrate except an end portion of the drain electrode; forming a transparent conducting oxide layer an entire of the substrate and a negative photoresist on the transparent conducting oxide layer; performing a back exposure to the negative photoresist; and forming a pixel electrode by way of patterning the negative photoresist after the back exposure and by way of photolithography process, wherein the pixel electrode is disposing in a pixel region and contacting the drain electrode.

The transparent conducting oxide layer is a material selected from a group consisting of indium tin oxide and indium zinc oxide. The method further includes etching a portions of the doped amorphous silicon layer of the active layer to form a channel region between the source and drain electrodes.

Hereinafter, reference will now be made in detail to the preferred embodiment of the present invention, example of which is illustrated in the accompanying drawings.

Fig. 6 is a plan view illustrating a pixel of a thin film transistor (TFT) array substrate for use in a liquid crystal display (LCD) panel according to the principles of the present invention. A gate line 100 is arranged in a transverse direction and a data line 110 is arranged in a direction perpendicular to the gate line 110. A gate pad 106 is located at one end of the gate line 100 and a gate pad electrode 108 is formed on the gate pad 106. A data pad 118 is positioned at one end of the data line 110 and a data pad electrode 120 is formed on the data pad 118.

A gate electrode 102 that extends from the gate line 100 is positioned near the crossing of the gate and data lines 100 and 110. A source electrode 114 extends from the data line 110 near that crossing and over the gate electrode 102. A drain electrode 116 is formed spaced apart from the source electrode 114 and over the gate electrode 102. Thus, a thin film transistor (TFT), which includes the gate electrode 102 and the source and drain electrodes 114 and 116, is positioned at a predetermined crossing location of the gate and data lines 100 and 110.

Further, a protection layer 112 is positioned so as to protect the TFT and the data line 110. A pixel electrode 130 having an electrical contact with the drain electrode 116 is then formed. Significantly, the pixel electrode 130 is connected to a side portion of the drain electrode 116. Thus, a drain contact hole is not needed through the protection layer 112 as in the prior art. The side portion of the drain electrode 116 beneficially has a bent-shaped periphery. This bent-shaped periphery enables an increase in the contact area between the drain electrode 116 and the pixel electrode 130.

Figs. 7A to 7D are cross-sectional views taken along a line VII-VII of Fig. 6 and help illustrate the steps of fabricating a TFT array substrate according to the present invention. In the embodiment of the present invention, the pixel electrode 130 (see Fig. 6) is formed using only the back exposure, and the pixel electrode is in contact with the side portion of the drain electrode, i.e., a side contact is used.

Fig. 7A shows a step for forming the gate electrode 102 on a substrate 1 by patterning a first metal layer. As a metal for the gate electrode 102, Aluminum, Chrome or Molybdenum is beneficially used.

Referring to Fig. 7B, the gate insulation layer 150 is formed over the surface of the substrate 1, especially over the gate electrodes 102. Then, a pure amorphous silicon (a-Si:H)

layer and a doped amorphous silicon (n+ a-Si:H) layer are sequentially formed on the gate insulation layer 150 and then patterned to form a semiconductor layer 152 that includes an active layer and an ohmic contact layer.

As depicted in Fig. 7C, the source and drain electrodes 114 and 116 are then formed by depositing and patterning a second metal layer. A portion of the upper layer of the semiconductor layer 152 (i.e., the ohmic contact layer) is etched to form a channel region CH using the source and drain electrodes 114 and 116 as masks.

As shown in Fig. 7D, a protection layer 112 is formed to protect the channel region CH. This is performed by depositing an insulation material over the substrate structure. That insulation material is then etched to expose a side portion of the drain electrode 116. That side portion will be used to connect the drain electrode 116 to the pixel electrode 130, which is formed in a later step.

Fig. 7D also shows a step of sequentially depositing a Transparent Conducting Oxide (TCO) 130a and a photoresist 156. Indium Tin Oxide (ITO) or Indium Zinc Oxide (IZO) is usually employed for the Transparent Conducting Oxide (TCO) layer 130a. The photoresist 156 is a material which, when subjected to light irradiation through a mask, absorbs light energy and undergoes a photochemical reaction to form a latent image. To get a high aperture ratio, a negative photoresist is used according to this embodiment of the invention. The portion of the photoresist which does not absorb light is removed during a developing process. A back exposure is used in the patterning process to enhance the aperture ratio. The back exposure is performed to form the pixel electrode 130. As shown in Fig. 7D, an exposed portion of the photoresist 156 is exposed by the back exposure, and a non-exposed portion of the photoresist 156 is not exposed by the back exposure. Thus, the portion of the TCO layer

130a which is under the exposed portion of the photoresist 156 is defined as the pixel electrode 130 (see Fig. 8).

Fig. 8 shows a cross-sectional view of a completed substrate according to the embodiment of the present invention. The high aperture ratio is materialized by the back exposure due to the fact that the area of the pixel electrode is enlarged, i.e., there is no gap between the data line 110 and the pixel electrode 130.

Referring to Fig. 9, which is an isolated view of a portion H of Fig. 8, the drain electrode 116 and the pixel electrode 130 have side contacts with each other. In the conventional method, the back exposure and a front exposure are used to connect the drain electrode to the pixel electrode. However, according to the embodiment of the present invention, since the side portion of the drain electrode 116 is exposed by the protection layer 112, the pixel electrode 130 can be connected to the drain electrode 116 by being patterned using back exposure without the front exposure. Thus, the additional mask process for the front exposure is not required.

Meanwhile, as shown in Fig. 9, the pixel electrode 130 overlaps the portion of the drain electrode 116 by a distance of about 2 micrometers. This is attained by a diffraction effect of the light during the back exposure and by the patterning processes. Thus, the distance of the overlapped portion between the pixel electrode 130 and the drain electrode 116 can be controlled to about 2 micrometers. In the embodiment of the present invention, the distance of the overlapped portion between the drain electrode 116 and the pixel electrode 130 increases the contact area when compared to the contact area of using only the side portion of the drain electrode 116. Also in the present invention, the overlapped portion of the drain electrode 116 and the pixel electrode 130 can be 0.5 micrometers in order to decrease a contact resistance between the drain electrode 116 and the pixel electrode 130

Fig. 10 is a cross-sectional view taken along a line IX-IX of Fig. 6 and illustrates a gate pad 106 and a data pad 118 according to the present embodiment. When forming the gate pad electrode 108 and the data electrode 120, a back exposure similar to or same as that used to form the pixel electrode 130 is adopted. The overlapped portions between the gate pad 106 and gate pad electrode 108, and between the data pad 118 and the data pad electrode 120, can be a distance of about 0.5 to 2 micrometers.

Fig. 11 is a plan view illustrating a gate pad 106 or a data pad 118. Gate pad or data pad openings are formed before forming the gate pad electrode 108 or the data pad electrodes 120. In this process, the number of the pad openings formed in an individual pad can be more than one, and the pad openings can have bent-shaped peripherals in order to increase the contact area.

As mentioned above, the present invention is fabricated using only four-masks, and a high aperture ratio is achieved by forming the pixel electrode using back exposure. Specifically, a front exposure is not needed to connect the pixel electrode to the drain electrode. Moreover, by forming numerous pad openings and bent-shaped opeings the contact area between the pad electrodes and the pads can be increased.

It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

[EFFECT OF INVENTION]

Accordingly, the TFT substrate of the illustrated embodiment has the following advantages.

First, since the illustrated embodiment of the present invention employs a four-mask process, the TAT (turn around time) or time of production can be reduced.

Second, due to the four-mask process, the manufacturing yelds can increase because mis-alignment can be reduced.

Third, because of the reduced number of process steps, the cost of production can be decreased.

Fourth, because the pixel electrode is formed using only back exposure, a high aperture ratio can be achieved.

Fifth, because the gate and data pads have the bent-shaped openings, the pad electrodes can have the increase contact areas with the gate and data pads.

[RANGE OF CLAIMS]

[CLAIM 1]

An array substrate for use in a liquid crystal display device, comprising:

a substrate having a pixel region and a switching region at one corner of the pixel region;

a gate line arranged in a transverse direction on the substrate, a gate electrode extending from the gate line into the switching region, a gate pad at the end of the gate line, and a gate pad electrode over the gate pad;

a data line perpendicularly crossing the gate line to define the pixel region, a source electrode extending from the data line over a portion of the gate electrode in the switching region, a data pad at the end of the data line, and a data pad electrode over the data pad;

a drain electrode opposite and corresponding to the source electrode in the switching region and overlapping a portions of the gate electrode;

a protection layer overlapping the gate electrode, the source electrode, and the drain electrode, and exposing one end portion of the drain electrode; and

a pixel electrode contacting the end portion of the drain electrode and disposing over an entire of the pixel region.

[CLAIM 2]

The array substrate according to claim 1, wherein the end portion of the drain electrode has a prominence and depression shape.

[CLAIM 3]

The array substrate according to claim 1, wherein the gate pad includes a gate pad opening and wherein the gate pad electrode contacts side portions of the gate pad in the gate pad opening.

[CLAIM 4]

The array substrate accroding to claim 1, wherein the data pad includes a gate pad opening and wherein the data pad electrode contacts side portions of the data pad in the data pad opening.

[CLAIM 5]

The array substrate according to either of claims 3 and 4, wherein each of the gate and data pad openings has a prominence and depression shape.

[CLAIM 6]

An array substrate for use in a liquid crystal display device, comprising:

a substrate;

a gate electrode formed on the substrate;

a gate insulation layer on the substrate to cover the gate electrode;

an active layer on the gate insulation layer and over the gate electrode;

source and drain electrodes contacting the active layer;

a protection layer covering the active layer and the source electrode, and exposing a portion of the drain electrode; and

a pixel electrode contacting side portions of the drain electrode.

[CLAIM 7]

The array substrate according to claim 6, wherein the pixel electrode overlaps the side portions of the drain electrode by a distance of less than 2 micrometers.

[CLAIM 8]

A method of forming an array substrate for use in a liquid crystal display device, comprising:

providing a substrate;

forming a gate electrode on the substrate;

forming a gate insulation layer on the substrate to cover the gate electrode;

forming an active layer on the gate insulation layer and above the gate electrode, wherein the active layer includes a pure amorphous silicon layer and a doped amorphous silicon layer;

forming source and drain electrodes on the active layer;

forming a channel region between the source and drain electrodes;

forming a protection layer over an entire of the substrate except an end portion of the drain electrode;

forming a transparent conducting oxide layer an entire of the substrate and a negative photoresist on the transparent conducting oxide layer;

performing a back exposure to the negative photoresist; and

forming a pixel electrode by way of patterning the negative photoresist after the back exposure and by way of photolithography process, wherein the pixel electrode is disposing in

a pixel region and contacting the drain electrode.

[CLAIM 9]

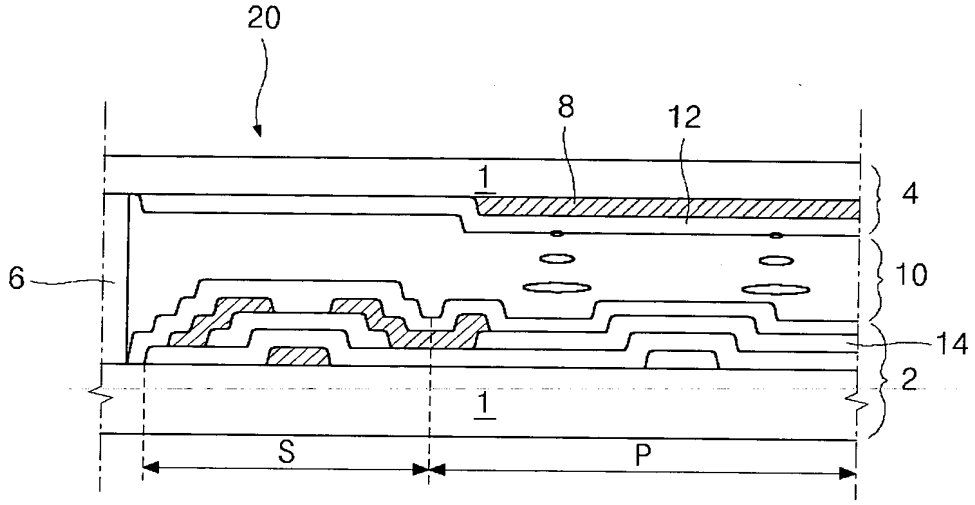
The array substrate according to claim 8, wherein the transparent conducting oxide layer is a material selected from a group consisting of indium tin oxide and indium zinc oxide.

[CLAIM 10]

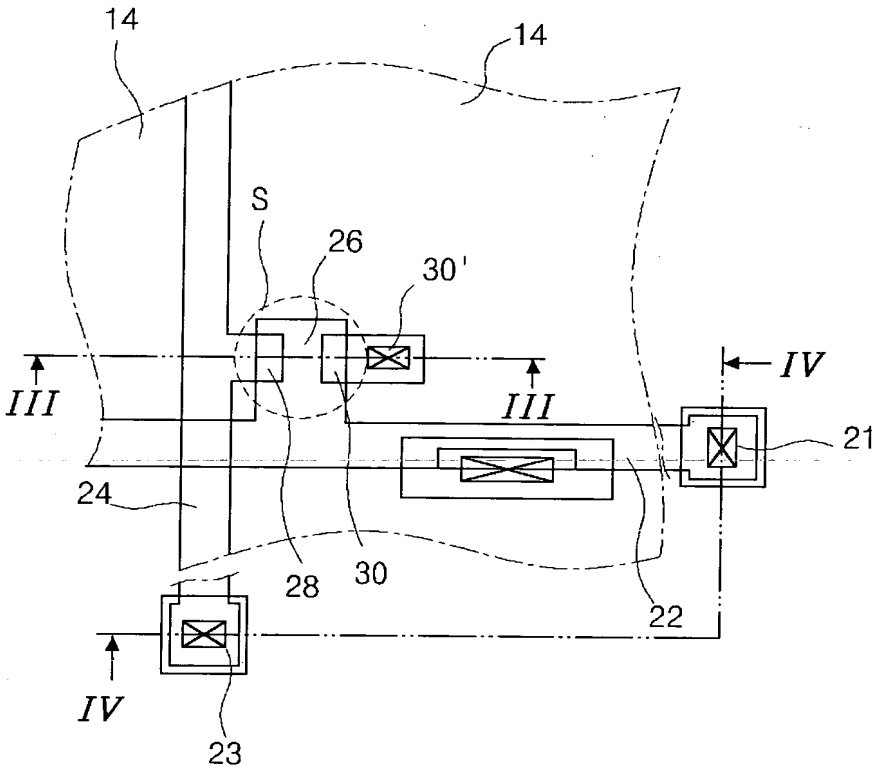
The array substrate according to claim 8, further comprising etching a portions of the doped amorphous silicon layer of the active layer to form a channel region between the source and drain electrodes.

[DRAWINGS]

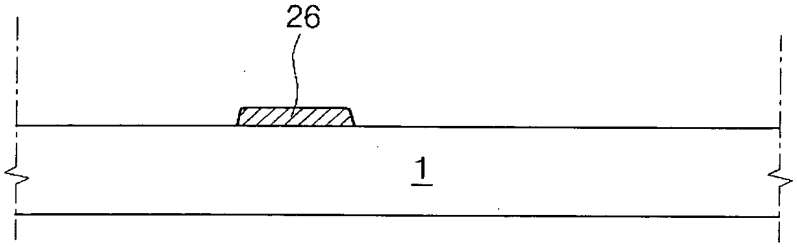
[Fig. 1]



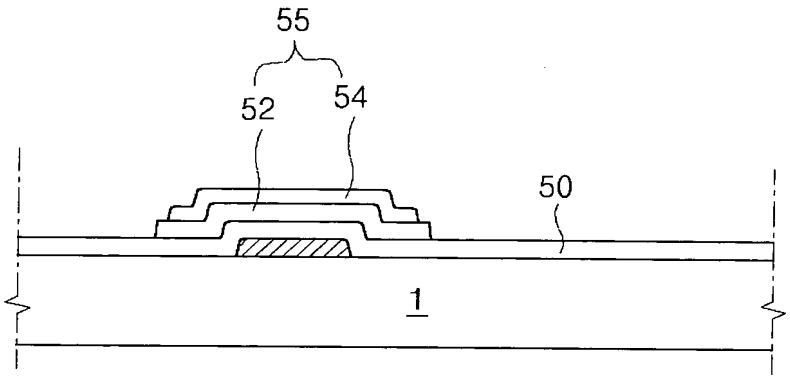
[Fig. 2]



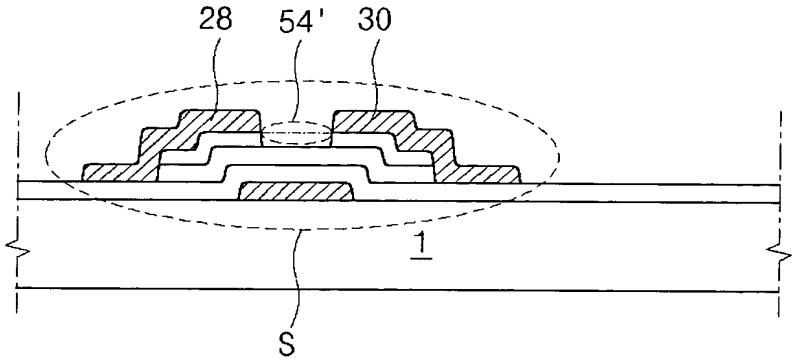
[Fig. 3A]



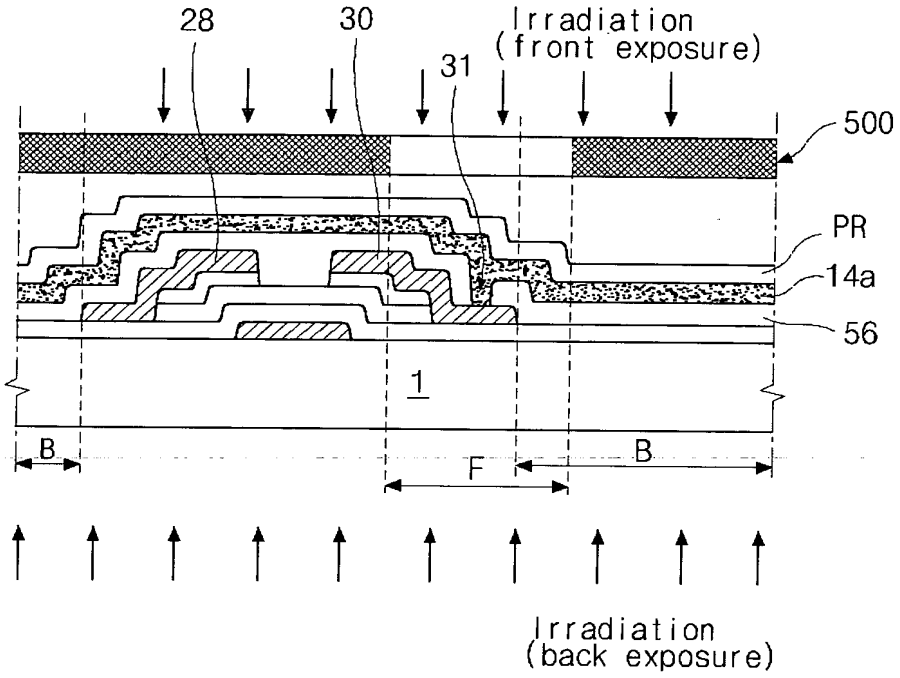
[Fig. 3B]



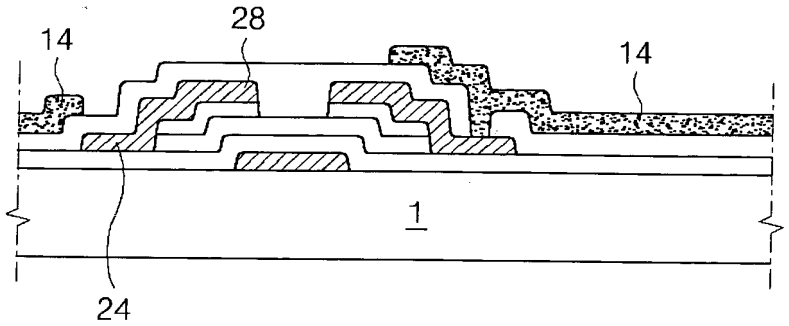
[Fig. 3C]



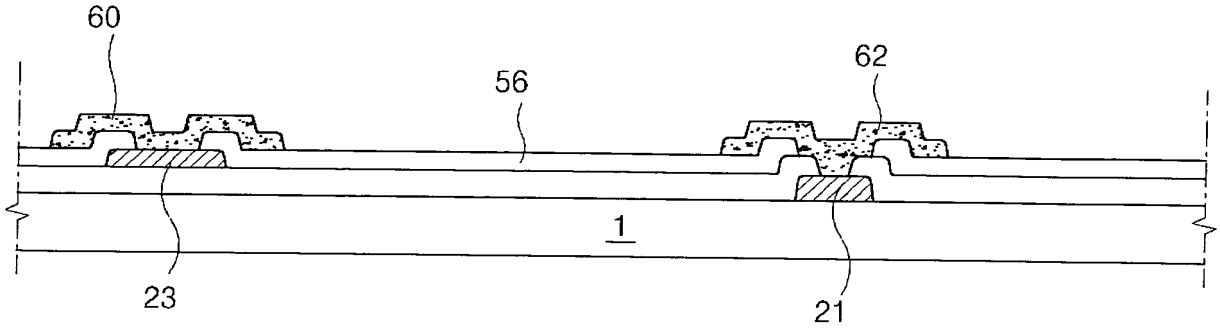
[Fig. 3D]


28
30
31
Irradiation
(front exposure)
500
PR
14a
56
1
B
F
B
Irradiation
(back exposure)

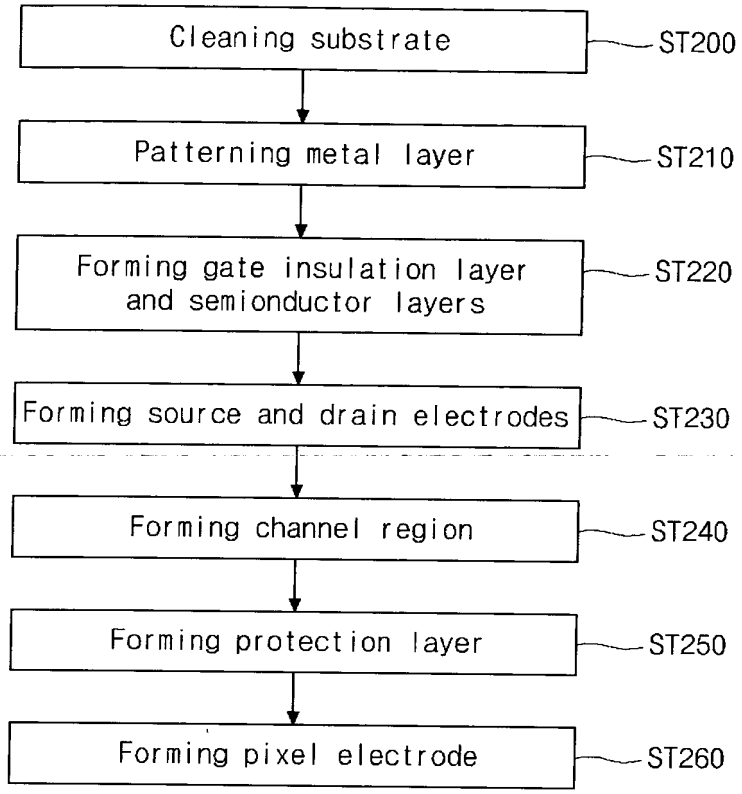
[Fig. 3E]



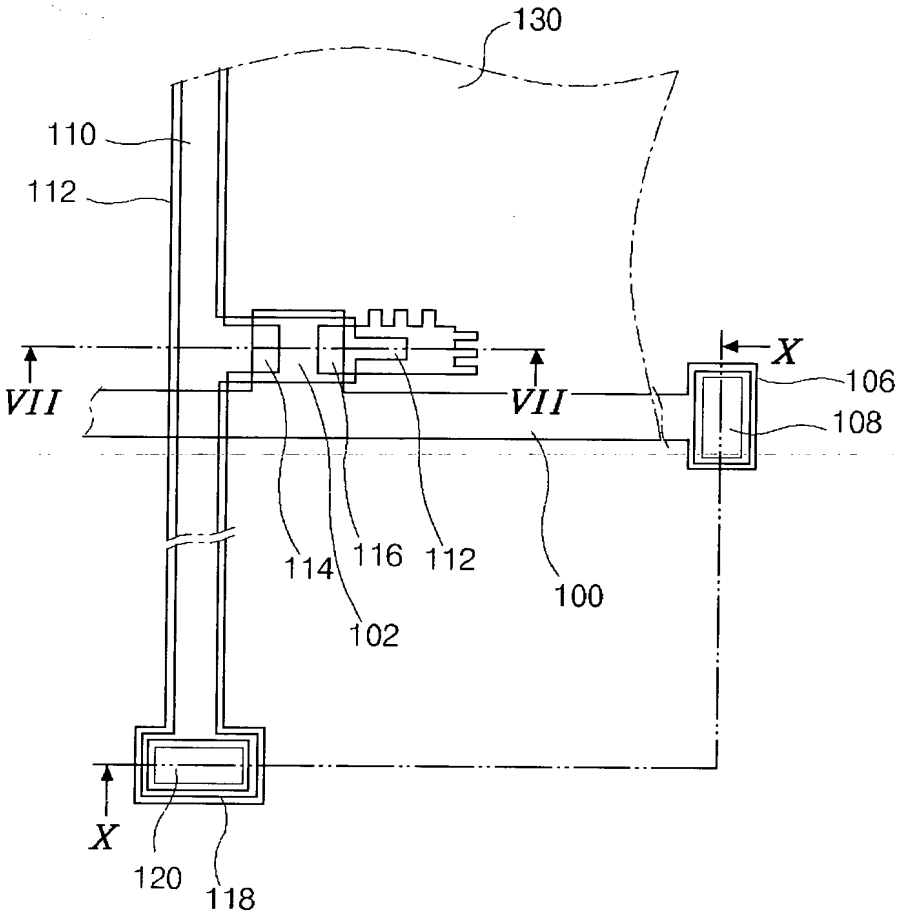
[Fig. 4]



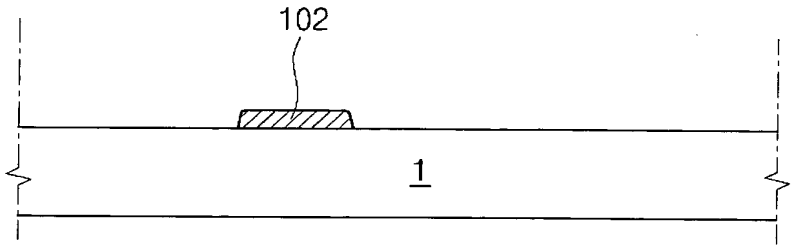
[Fig. 5]


Cleaning substrate
ST200
Patterning metal layer
ST210
Forming gate insulation layer and semionductor layers
ST220
Forming source and drain electrodes
ST230
Forming channel region
ST240
Forming protection layer
ST250
Forming pixel electrode
ST260

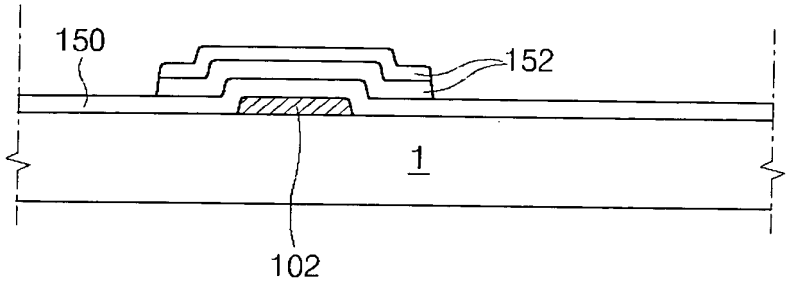
[Fig. 6]



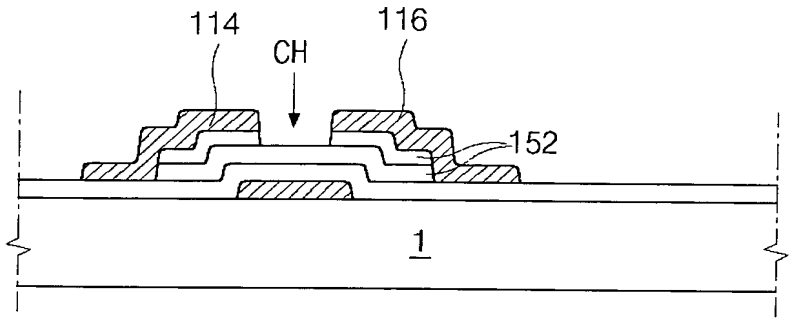
[Fig. 7A]



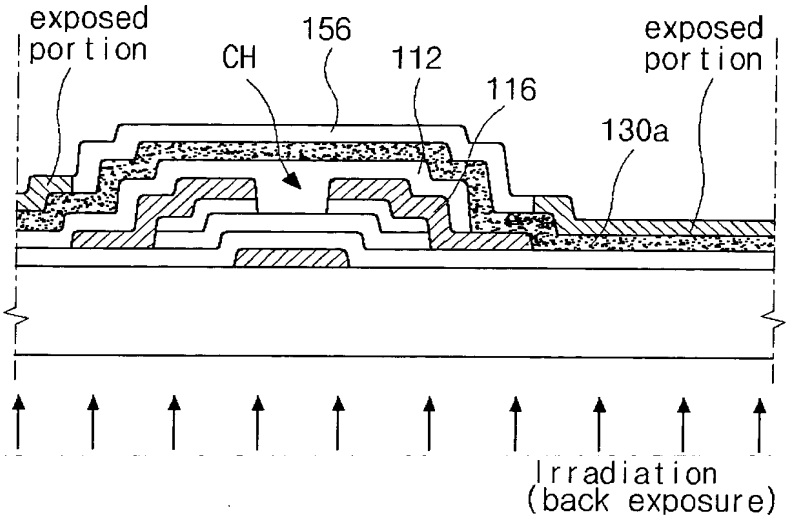
[Fig. 7B]



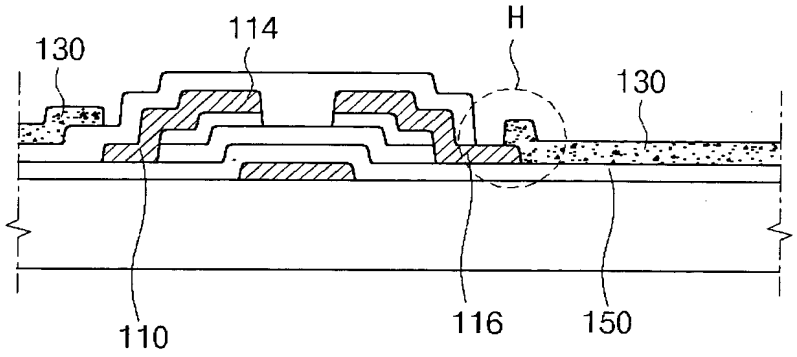
[Fig. 7C]



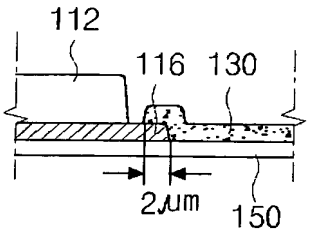
[Fig. 7D]


exposed portion
CH
156
112
116
130a
exposed portion
Irradiation (back exposure)

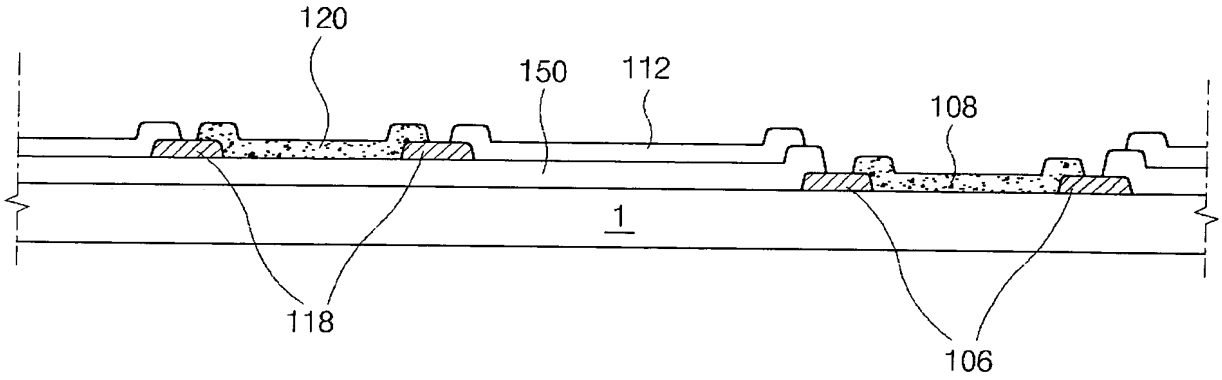
[Fig. 8]



[Fig. 9]



[Fig. 10]



[Fig. 11]